

Application No.: 10/696,588
Amendment Under 37 C.F.R. §1.111 dated May 16, 2005
Reply to the Office Action dated February 22, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Currently Amended): A method for manufacturing a semiconductor device including steps of forming a wiring by a dual damascene method, the method for manufacturing the semiconductor device comprising the steps of:

forming a cap film, a first interlayer insulating film, an etching stopper film, a second interlayer insulating film, and a hard mask in this order on a conductive layer;

forming a via hole which reaches the cap film in the hard mask, the second interlayer insulating film, the etching stopper film, and the first interlayer insulating film;

embedding an embedded material to a level higher than the first interlayer insulating film, and lower than the top surface of a layered stack composed of the first interlayer insulating film, the etching stopper film, and the second interlayer insulating film in the via hole;

forming a trench whose bottom is above ~~higher than~~ an upper surface of the etching stopper film and below ~~lower than that of~~ the embedded material in the second interlayer insulating film by etching the hard mask and the second interlayer insulating film, using a resist mask in which an opening for exposing the embedded material is formed;

removing the resist mask and the embedded material;

etching the second interlayer insulating film again by using the hard mask as a mask;

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forming a wiring trench by removing the hard mask, and exposed parts of the etching stopper film, and the cap film; and
embedded an electric conductive film in the via hole and the wiring trench.

Claim 2 (Original): The method for manufacturing the semiconductor device according to claim 1, wherein

a height of the embedded material is adjusted in said step of embedding the embedded material so that a bottom of the trench is lower than the upper surface of the embedded material even if the embedded material is etched when etching the hard mask and the second interlayer insulating film.

Claim 3 (Original): The method for manufacturing the semiconductor device according to claim 1, wherein

the first and the second interlayer insulating films are SiOC group insulation films.

Claim 4 (Original): The method for manufacturing the semiconductor device according to claim 2, wherein

the first and the second interlayer insulating films are SiOC group insulation films.

Claim 5 (Original): The method for manufacturing the semiconductor device according to claim 1, wherein

the etching stopper film and the hard mask are made of an identical material.

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Claim 6 (Original): The method for manufacturing the semiconductor device according to claim 2, wherein

the etching stopper film and the hard mask are made of an identical material.

Claim 7 (Original): The method for manufacturing the semiconductor device according to claim 3, wherein

the etching stopper film and the hard mask are made of an identical material.

Claim 8 (Original): The method for manufacturing the semiconductor device according to claim 4, wherein

the etching stopper film and the hard mask are made of an identical material.

Claim 9 (Original): The method for manufacturing the semiconductor device according to claim 1, wherein

the cap film, the etching stopper film and the hard mask are made of materials capable of being removed under an identical etching condition.

Claim 10 (Original): The method for manufacturing the semiconductor device according to claim 2, wherein

the cap film, the etching stopper film and the hard mask are made of materials capable of being removed under an identical etching condition.

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Claim 11 (Original): The method for manufacturing the semiconductor device according to claim 3, wherein

the cap film, the etching stopper film and the hard mask are made of materials capable of being removed under an identical etching condition.

Claim 12 (Original): The method for manufacturing the semiconductor device according to claim 4, wherein

the cap film, the etching stopper film and the hard mask are made of materials capable of being removed under an identical etching condition.

Claim 13 (Original): The method for manufacturing the semiconductor device according to claim 5, wherein

the cap film, the etching stopper film and the hard mask are made of materials capable of being removed under an identical etching condition.

Claim 14 (Original): The method for manufacturing the semiconductor device according to claim 6, wherein

the cap film, the etching stopper film and the hard mask are made of materials capable of being removed under an identical etching condition.

Claim 15 (Original): The method for manufacturing the semiconductor device according to claim 7, wherein

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the cap film, the etching stopper film and the hard mask are made of materials capable of being removed under an identical etching condition.

Claim 16 (Original): The method for manufacturing the semiconductor device according to claim 8, wherein

the cap film, the etching stopper film and the hard mask are made of materials capable of being removed under an identical etching condition.

Claim 17 (Currently Amended): A method for manufacturing a semiconductor device according to claim 1, wherein

~~said step of embedded the electric conductive film in the via hole and the wiring trench.~~
includes the step of:

including steps of forming a wiring by a dual damascene method, the method for manufacturing the semiconductor device comprising the steps of:

forming a cap film, a first interlayer insulating film, an etching stopper film, a second interlayer insulating film, and a hard musk in this order on a conductive layer;

forming a via hole which reaches the cap film in the hard musk, the second interlayer insulating film, the etching stopper film, and the first interlayer insulating film;

embedding an embedded material to a level higher than the first interlayer insulating film and lower than the top surface of a layered stack composed of the first interlayer insulating film, the etching stopper film, and the second interlayer insulating film in the via hole;

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forming a trench whose bottom is above an upper surface of the etching stopper film and below that of the embedded material in the second interlayer insulating film by etching the hard mask and the second interlayer insulating film, using a resist mask in which an opening for exposing the embedded material is formed;

removing the resist mask and the embedded material;

etching the second interlayer insulating film again by using the hard mask as a mask;

forming a wiring trench by removing the hard mask, and exposed parts of the etching stopper film, and the cap film;

forming a barrier metal film on the surface of the via hole and the wiring trench; and

forming a wiring material on the barrier metal film.

Claim 18 (Original): The method for manufacturing the semiconductor device according to claim 2, wherein

said step of embedding the electric conductive film in the via hole and the wiring trench includes the steps of:

a step of forming a barrier metal film on the surface of the via hole and the wiring trench;

and

a step of forming a wiring material on the barrier metal film.

Claim 19 (Original): The method for manufacturing the semiconductor device according to claim 17, wherein

said step of forming the wiring material includes the steps of:

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forming a seed film on the barrier metal film; and
forming a metal film on the seed film by a plating method.

Claim 20 (Original): The method for manufacturing the semiconductor device according to claim 18, wherein

said step of forming the wiring material includes the steps of:
forming a seed film on the barrier metal film; and
forming a metal film on the seed film by a plating method.

Claim 21 (New): A method for manufacturing a semiconductor device including steps of forming a wiring by a dual damascene method, the method for manufacturing the semiconductor device comprising the steps of:

forming a cap film, a first interlayer insulating film, an etching stopper film, a second interlayer insulating film, and a hard mask in this order on a conductive layer;

forming a via hole which reaches the cap film in the hard mask, the second interlayer insulating film, the etching stopper film, and the first interlayer insulating film;

embedding an embedded material in the via hole;

forming a trench whose bottom is above an upper surface of the etching stopper film and below that of the embedded material in the second interlayer insulating film by etching the hard mask and the second interlayer insulating film, using a resist mask in which an opening for exposing the embedded material is formed;

removing the resist mask and the embedded material;

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etching the second interlayer insulating film again by using the hard mask as a mask;

forming a wiring trench by removing the hard mask, and exposed parts of the etching stopper film, and the cap film; and

embedded an electric conductive film in the via hole and the wiring trench.